VLSI FRONTEND 2017-16 Projects List

S.No	PAPER ID	IEEE TITLE	YEAR
1	STVS001	A Cost and Power Efficient Image Compressor VLSI Design with Fuzzy Decision and Block Partition for Wireless Sensor Networks	2017
2	STVS002	A Hardware-Efficient Scalable Spike Sorting Neural Signal Processor Module for Implantable High-Channel-Count Brain Machine Interfaces	2017
3	STVC083	A Low-Voltage Radiation-Hardened 13T SRAM Bitcell for Ultralow Power Space Applications	2017
4	STVS003	A Memory-Based FFT Processor Design With Generalized Efficient Conflict-Free Address Schemes	2017
5	STVS004	AES Datapath Optimization Strategies for Low-Power Low-Energy Multisecurity-Level Internet-of-Thing Applications	2017
6	STVS005	AN FFT-BASED SYNCHRONIZATION APPROACH TO RECOGNIZE HUMAN BEHAVIORS USING STN-LFP SIGNAL	2017
7	STVS006	An FPGA based High Speed Error resilient Data aggregation and control for High Energy Physics Experiment	2017
8	STVS007	Automatic Generation of High-Performance Modular Multipliers for Arbitrary Mersenne Primes on FPGAs	2017
9	STVS008	Compressed FEC Codes with Spatial-Coupling	2017
10	STVS009	Coordinate Rotation-Based Low Complexity K-Means Clustering Architecture	2017
11	STVS010	Decimal Floating-Point Multiplier With Binary- Decimal Compression Based Fixed-Point Multiplier	2017
12	STVS011	Efficient FPGA Mapping of Pipeline SDF FFT Cores	2017
13	STVS012	HARDWARE-BASED LINEAR PROGRAMMING DECODING VIA THE ALTERNATING DIRECTION METHOD OF MULTIPLIERS	2017
14	STVS013	Implementation of Multiplier Architecture Using Efficient Carry Select adders for synthesizing FIR filters	2017
15	STVS014	Layered Constructions for Low-Delay Streaming Codes	2017
16	STVS015	Low-Latency, Low-Area, and Scalable Systolic-Like Modular Multipliers for GF(2m) Based on Irreducible All-One Polynomials	2017
17	STVS016	Multipliers-Driven Perturbation of Coefficients for Low-Power Operation in Reconfigurable FIR Filters	2017
18	STVS017	Performance Analysis of LDPC-Based RFID Group Coding	2017
19	STVS018	Practical Dirty Paper Coding Schemes Using One Error Correction Code with Syndrome	2017

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S.No	PAPER ID	IEEE TITLE	YEAR
20	STVC106	Recursive Approach to the Design of a Parallel Self-Timed Adder	2017
21	STVC080	0.7-V Three-Stage Class-AB CMOS Operational Transconductance Amplifier	2016
22	STVC094	A 0.45-V Low-Power OOK/FSK RF Receiver in 0.18 µm CMOS Technology for Implantable Medical Applications	2016
23	STVC053	A 14-bit 250 MS/s IF Sampling Pipelined ADC in 180 nm CMOS Process	2016
24	STVC077	A 40–170 MHz PLL-Based PWM Driver Using2-/3-/5-Level Class-D PA in 130 nm CMOS	2016
25	STVC008	A 6 b 5 GS/s 4 Interleaved 3 b/Cycle SAR ADC	2016
26	STVC064	A Compact One-Pin Mode Transition Circuit forClock Synchronization in Current-Mode Controlled Switching Regulators	2016
27	STVC035	A Computationally Efficient Reconfigurable FIR Filter Architecture Based on Coefficient	2016
28	STVC018	A Configurable Parallel Hardware Architecture for Efficient Integral Histogram Image Computing	2016
29	STVS020	A Dynamically Reconfigurable Multi-ASIP Architecture for Multistandard and Multimode Turbo Decoding	2016
30	STVC048	A Fully Digital Front-End Architecture for ECG Acquisition System With 0.5 V Supply	2016
31	STVS031	A Generalized Algorithm and ReconfigurableArchitecture for Efficient and Scalable OrthogonalApproximation of DCT	2016
32	STVS022	A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications	2016
33	STVC025	A High-Throughput Energy-Efficient Implementation of Successive Cancellation Decoder for Polar Codes Using Combinational Logic	2016
34	STVC046	A Low Power Class-AB Audio Power Amplifier With Dynamic Transconductance Compensation in 55 nm CMOS Process	2016
35	STVC017	A Low-Power Broad-Bandwidth Noise Cancellation VLSI Circuit Design for In-Ear Headphones	2016
36	STVC056	A Low-Power Class-AB Gm-Based Amplifier With Application to an 11-bit Pipelined ADC	2016
37	STVC042	A Low-Power Oscillator-Based Readout Interface for Medical Ultrasonic Sensors	2016
38	STVC011	A Low-Power Robust Easily CascadedPentaMTJ-Based Combinational and Sequential Circuits	2016
39	STVS032	A Mixed-Decimation MDF Architecture for Radix-2 kParallel FFT	2016
40	STVC002	A New XOR-Free Approach for Implementation of Convolutional Encoder	2016

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41	STVC022	A Normal I/O Order Radix-2 FFT Architecture to Process Twin Data Streams for MIMO	2016
42	STVS024	A Novel Coding Scheme for Secure Communications in Distributed RFID Systems	2016
43	STVC020	A Novel Quantum-Dot Cellular Automata {X} -bit \times 32 -bit SRAM	2016
44	STVC095	A Process-Tolerant, Low-Voltage, Inverter-Based OTA for Continuous-Time sigma	2016
45	STVC079	A Short-Channel-Effect-Degraded Noise Margin Model for Junctionless Double-Gate MOSFET Working on Subthreshold CMOS Logic Gates	2016
46	STVC054	A Simple And Reliable System To Detect And Correct setup/Hold Time Violations In Digital Circuits	2016
47	STVC098	A Simple FPGA System for ECG R-R Interval Detection	2016
48	STVC001	A Single-Ended With Dynamic Feedback Control 8T Subthreshold SRAM Cell	2016
49	STVC099	A Thermal Energy Harvesting Power Supply With an Internal Startup Circuit for Pacemakers	2016
50	STVC091	Achieving Optimal Efficiency in Energy Transfer to a CMOS Fully Integrated Wireless Power Receiver	2016
51	STVC012	Algorithm and Architecture of Configurable Joint Detection and Decoding for MIMO Wireless Communications With Convolutional Codes	2016
52	STVC085	An active merchant balun and its application to a 24-ghz cmos mixer	2016
53	STVC071	An Area and Power Efficient Adder-Based Stepwise Linear Interpolation for Digital Signal Processing	2016
54	STVC045	An Area-Efficient High-Resolution Resistor-String DAC with Reverse Ordering Scheme for Active Matrix Flat-Panel Display Data Driver Ics	2016
55	STVS019	An Efficient Constant Multiplier Architecture Based on Vertical-Horizontal Binary Common Sub-expression Elimination Algorithm for Reconfigurable FIR	2016
56	STVC014	An Efficient Hybrid-Swi tched Network-on-Chip for Chip Multiprocessors	2016
57	STVC092	An Efficient On-Chip Switched-Capacitor-Based Power Converter for a Microscale Energy Transducer	2016
58	STVC007	An Efficient Single and Double-Adjacent Error Correcting Parallel Decoder for the (24,12) Extended Golay Code	2016
59	STVS028	An MPCN-Based BCH Codec Architecture With Arbitrary Error Correcting Capability	2016
60	STVS041	An Optimized Modified Booth Recoder for Efficient Design of the Add-Multiply Operator	2016
61	STVC062	Analysis and Design of an E-Band Transformer-Coupled Low-Noise Quadrature VCO in 28-nm CMOS	2016

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62	STVC049	Analysis and Design of an Ultrabroadband Stacked Power Amplifier in CMOS Technology	2016
63	STVC058	Analysis and Optimization of Product-Accumulation Section for Efficient Implementation of FIR Filters	2016
64	STVC050	Approximate Radix-8 Booth Multipliers for Low-Power and High-Performance Operation	2016
65	STVC015	Architecture of a Reusable BIST Engine for Detection and Autocorrection of Memory Failures and for IO Debug, Validation, Link Training, and Power Optimization on 14-nm SoC	2016
66	STVC093	Bit-Interleaving-Enabled 8T SRAM With Shared Data-Aware Write and Reference-Based Sense Amplifier	2016
67	STVC024	Built-In Self-Test and Digital Calibration of Zero-IF RF Transceivers	2016
68	STVC090	Built-In Self-Test Methodology With Statistical Analysis for Electrical Diagnosis of Wearout in a Static Random Access Memory Array	2016
69	STVC074	CMCS: Current-Mode Clock SynthesisII	2016
70	STVC097	CMOS Integrated Time-Mode Temperature Sensor for Self-Refresh Control in DRAM Memory Cell	2016
71	STVC016	Comments on and corrections to ‘ unified VLSI architecture for photo core transform used in JPEG XR	2016
72	STVC066	Compensation Method for Multistage Opamps With High Capacitive Load Using Negative Capacitance	2016
73	STVC004	Computing Seeds for LFSR-Based Test Generation From Nontest Cubes	2016
74	STVS026	Concept, Design, and Implementation of Reconfigurable CORDIC	2016
75	STVS039	DESIGN AND IMPLEMENTATION OF FAST FLOATING POINT MULTIPLIER UNIT	2016
76	STVC061	Design and Analysis of a Highly Efficient Linearized CMOS Subharmonic Mixer for Zero and Low-IF Applications	2016
77	STVC069	Design of a CMOS System-on-Chip for Passive, Near-Field Ultrasonic Energy Harvesting and Back-Telemetry	2016
78	STVC082	Design of an offset-tolerant voltage sense amplifier bit-line sensing circuit for SRAM memories	2016
79	STVC038	Design of QPP Interleavers for the ParallelTurbo Decoding Architecture	2016
80	STVC063	Design-Efficient Approximate Multiplication Circuits Through Partial Product Perforation	2016
81	STVC028	Detection of Superpoints Using a Vector Bloom Filter	2016
82	STVC031	Distributed Sensor Network-on-Chip for Performance Optimization of Soft-Error-Tolerant Multiprocessor System-on-Chip	2016

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83	STVC057	Dual Use of Power Lines for Design-for-Testability—A CMOS Receiver Design	2016
84	STVC041	Dual-Band Waveform Generator With Ultra-Wide Low-Frequency Tuning-Range	2016
85	STVS034	Dual-Scan Parallel Flipping Architecture for a Lifting-Based 2-D Discrete Wavelet Transform	2016
86	STVC070	Efficient 3-D Bus Architectures for Inductive-Coupling ThruChip Interfaces	2016
87	STVS036	Efficient Coding Schemes for Fault-Tolerant Parallel Filters	2016
88	STVC010	Energy and Area Efficient Three-Input XOR/ XNORs With Systematic Cell Design Methodology	2016
89	STVC076	Enhanced Built-In Self-Repair Techniques for Improving Fabrication Yield and Reliability of Embedded Memories	2016
90	STVS033	Enhanced Memory Reliability Against Multiple cell upsets using DMC	2016
91	STVS035	Fault Tolerant Parallel FFTs Using Error Correction Codes and Parseval Checks	2016
92	STVC027	Fixed-Point Computing Element Design for Transcendental Functions and Primary Operations in Speech Processing	2016
93	STVS038	Flexible DSP Accelerator Architecture Exploiting Carry-Save Arithmetic	2016
94	STVS037	Floating-Point Butterfly Architecture Based on Binary Signed-Digit Representation	2016
95	STVC073	Frequency-Boost Jitter Reduction for Voltage-Controlled Ring Oscillators	2016
96	STVC052	Fully Integrated 10-GHz Active Circulator and Quasi-Circulator Using Bridged-T Networks in Standard CMOS	2016
97	STVS040	Fully Reused VLSI Architecture of FM0/Manchester Encoding Using SOLS Technique for DSRC Applications	2016
98	STVC026	Glitch Energy Reduction and SFDR Enhancement Techniques for Low-Power Binary-Weighted Current-Steering DAC	2016
99	STVC043	Hard-Information Bit-Reliability Based Decoding Algorithm for Majority-Logic Decodable Nonbinary LDPC Codes	2016
100	STVC019	Hardware and Energy-Efficient StochasticLU Decomposition Scheme for MIMO Receivers	2016
101	STVC072	High sensitivity CMOS RF-DC converter in HF RFID Band	2016
102	STVC023	High-Performance Pipelined Architecture of Elliptic Curve Scalar Multiplication Over GF({2}^{m})	2016
103	STVC005	High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels	2016

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104	STVC044	High-Speed, Low-Power, and Highly Reliable Frequency Multiplier for DLL-Based Clock Generator	2016
105	STVS029	High-Throughput Finite Field Multipliers Using Redundant Basis for FPGA and ASIC Implementations	2016
106	STVC037	Hybrid LUT/Multiplexer FPGA Logic Architectures--XILINX	2016
107	STVC029	Improving Nested Loop Pipelining on Coarse-Grained Reconfigurable Architectures	2016
108	STVS021	In-Field Test for Permanent Faults in FIFO Buffers of NoC Routers	2016
109	STVC033	Input-Based Dynamic Reconfiguration of Approximate Arithmetic Units for Video Encoding	2016
110	STVS027	Low Power Compressor Based MAC Architecture for DSP Applications	2016
111	STVC003	Low-Cost High-Performance VLSI Architecture for Montgomery Modular Multiplication	2016
112	STVC021	Low-Power ECG-Based Processor for Predicting Ventricular Arrhythmia	2016
113	STVC104	Low-power half-select free single-ended 10 transistor SRAM cell	2016
114	STVS023	Low-Power Parallel Chien Search Architecture Using a Two-Step Approach	2016
115	STVC034	Low-Power Split-Radix FFT Processors Using Radix-2 Butterfly Units	2016
116	STVC036	Low-power technique for dynamic comparators	2016
117	STVC013	LUT Optimization for Distributed Arithmetic-B Block Least Mean Square Adaptive Filter	2016
118	STVC006	MACS: A Highly Customizable Low-Latency Communication Architecture	2016
119	STVC040	Memory-Reduced Turbo Decoding Architecture Using NII Metric Compression	2016
120	STVC084	Modeling and design of EMI-Immune opamps in 0.18-um CMOS technology	2016
121	STVC086	Multiple-Cell Reference Scheme for Narrow Reference Resistance Distribution in Deep Submicrometer STT-RAM	2016
122	STVC078	Multiplierless Unity-Gain SDF FFTs	2016
123	STVC051	New Low Glitch and Low Power DET Flip-Flops Using Multiple C-Elements	2016
124	STVS042	Non-Binary Orthogonal Latin Square Codes for a Multilevel Phase Charge Memory (PCM)	2016

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125	STVC068	Open-Loop Fractional Division Using a Voltage-Comparator-Based Digital-to-Time Converter	2016
126	STVC096	Optimized Active Single-Miller CapacitorCompensation With Inner Half-FeedforwardStage for Very High-Load Three-Stage OTAs	2016
127	STVC055	Optimized built in self repair for multiple memories	2016
128	STVC075	Partially Repeated SC-LDPC Codes for Multiple-Access Channel	2016
129	STVC030	Power/Energy Minimization Techniques for Variability-Aware High-Performance 16-nm 6T-SRAM	2016
130	STVC047	Precharge-Free, Low-Power Content-Addressable Memory	2016
131	STVS025	Pre-Encoded Multipliers Based on Non-Redundant Radix-4 Signed-Digit Encoding	2016
132	STVC065	Rapidly Tunable Dual-Comb RF Photonic Filter for Ultrabroadband RF Spread Spectrum Applications	2016
133	STVC067	Reducing Power, Leakage, and Area of Standard-Cell ASICs Using Threshold Logic Flip-Flops	2016
134	STVC087	Shield: A Reliable Networ k-on-Chip Router Architecture for Chip Multiprocessors	2016
135	STVC039	Single Bit-Line 7T SRAM Cell for Near-Threshold Voltage Operation With Enhanced Performance and Energy in 14 nm FinFET Technology	2016
136	STVC059	Single-Ended Schmitt-Trigger-Based Robust Low-Power SRAM Cell	2016
137	STVC032	Timing Error Tolerance in Small Core Designs for SoC Applications	2016
138	STVC088	Two 122-GHz Phase-Locked Loops in 65-nm CMOS Technology	2016
139	STVC081	Variation Tolerant Differential 8T SRAM Cell for Ultralow Power Applications	2016
140	STVS030	VLSI Computational Architectures for the Arithmetic Cosine Transform	2016
141	STVS043	VLSI Implementation of Fast Addition Using Quaternary Signed Digit Number System	2016
142	STVC060	Wide-Range Adaptive RF-to-DC Power Converter for UHF RFIDs	2016
143	STVC089	75 GBd InP-HBT MUX-DAC module for high-symbol-rate optical transmission	2015
144	STVC100	Fault Tolerant Parallel Filters Based on Error Correction Codes	2015
145	STVC103	Low-Power Clock Distribution Using a Current-Pulsed Clocked Flip-Flop	2015

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146	STVC009	Read Bitline Sensing and Fast Local Write-Back Techniques in Hierarchical Bitline Architecture for Ultralow-Voltage SRAMs	2015
147	STVC101	FPGA Based Implementation & Power Analysis of Parameterized Walsh Sequences	2014
148	STVC102	High throughput pipelined 2D Discrete cosine transform for video compression	2014
149	STVC105	Low-Power Pulse-Triggered Flip-Flop Design Based on a Signal Feed-Through Scheme	2014
150	STVC107	VLSI Architecture for delay efficient 32-bit Multiplier using Vedic Mathematic sutras	2013

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