## VLSI FRONTEND 2017-16 Projects List

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</tr>
<tr>
<td>S.No</td>
<td>PAPER ID</td>
<td>IEEE TITLE</td>
<td>YEAR</td>
</tr>
<tr>
<td>------</td>
<td>----------</td>
<td>---------------------------------------------------------------------------</td>
<td>------</td>
</tr>
<tr>
<td>125</td>
<td>STVC068</td>
<td>Open-Loop Fractional Division Using a Voltage-Comparator-Based Digital-to-Time Converter</td>
<td>2016</td>
</tr>
<tr>
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</tr>
<tr>
<td>127</td>
<td>STVC055</td>
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</tr>
<tr>
<td>128</td>
<td>STVC075</td>
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</tr>
<tr>
<td>130</td>
<td>STVC047</td>
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</tr>
<tr>
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<td>STVS025</td>
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</tr>
<tr>
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</tr>
<tr>
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<td>STVC067</td>
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</tr>
<tr>
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</tr>
<tr>
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</tr>
<tr>
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</tr>
<tr>
<td>139</td>
<td>STVC081</td>
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</tr>
<tr>
<td>140</td>
<td>STVS030</td>
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</tr>
<tr>
<td>141</td>
<td>STVS043</td>
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</tr>
<tr>
<td>142</td>
<td>STVC060</td>
<td>Wide-Range Adaptive RF-to-DC Power Converter for UHF RFID</td>
<td>2016</td>
</tr>
<tr>
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<td>STVC089</td>
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</tr>
<tr>
<td>144</td>
<td>STVC100</td>
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</tr>
<tr>
<td>145</td>
<td>STVC103</td>
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</tr>
<tr>
<td>S.No</td>
<td>PAPER ID</td>
<td>IEEE TITLE</td>
<td>YEAR</td>
</tr>
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<td>-----------------------------------------------------------------------------</td>
<td>------</td>
</tr>
<tr>
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<td>STVC009</td>
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</tr>
<tr>
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</tr>
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</tr>
<tr>
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<td>STVC105</td>
<td>Low-Power Pulse-Triggered Flip-Flop Design Based on a Signal Feed-Through Scheme</td>
<td>2014</td>
</tr>
<tr>
<td>150</td>
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</tr>
</tbody>
</table>